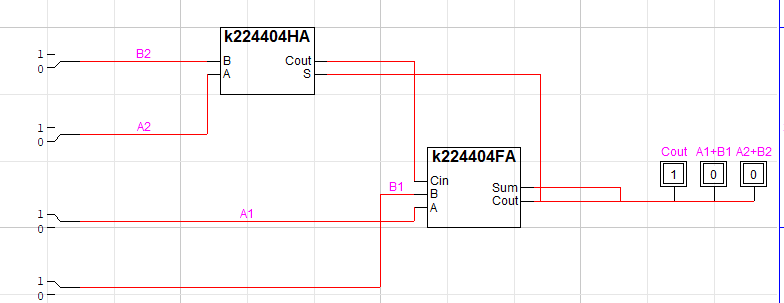
**In-Lab task Truth Table:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| A1 | A2 | B1 | B2 | Cout | S2 | S1 |
| 0 | **0** | **0** | **0** | **0** | **0** | **0** |
| 0 | **0** | **0** | **1** | **0** | **0** | **1** |
| 0 | **0** | **1** | **0** | **0** | **1** | **0** |
| 0 | **0** | **1** | **1** | **0** | **1** | **1** |
| 0 | **1** | **0** | **0** | **0** | **0** | **1** |
| 0 | **1** | **0** | **1** | **0** | **1** | **0** |
| 0 | **1** | **1** | **0** | **0** | **1** | **1** |
| 0 | **1** | **1** | **1** | **1** | **0** | **0** |
| 1 | **0** | **0** | **0** | **0** | **1** | **0** |
| 1 | **0** | **0** | **1** | **0** | **1** | **1** |
| 1 | **0** | **1** | **0** | **1** | **0** | **0** |
| 1 | **0** | **1** | **1** | **1** | **0** | **1** |
| 1 | **1** | **0** | **0** | **0** | **1** | **1** |
| 1 | **1** | **0** | **1** | **1** | **0** | **0** |
| 1 | **1** | **1** | **0** | **1** | **0** | **1** |
| 1 | **1** | **1** | **1** | **1** | **1** | **0** |

|  |  |
| --- | --- |
| INPUTS | OUTPUTS |

**In-Lab Task Circuit Diagram:**

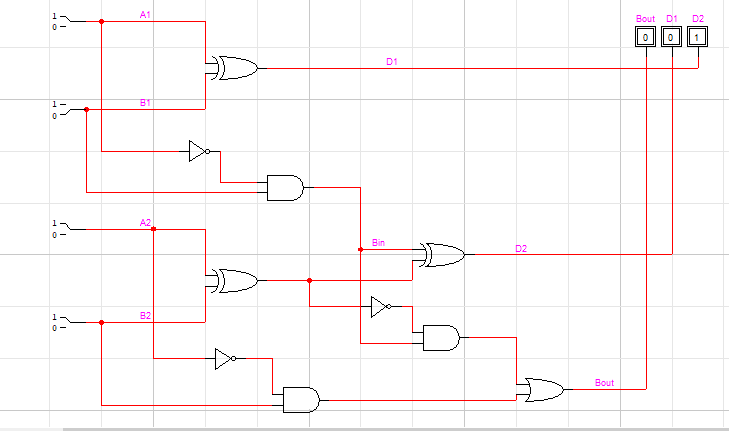


**Post-Lab Task 1 Truth Table:**

|  |  |
| --- | --- |
| INPUTS | OUTPUTS |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| A1 | A2 | B1 | B2 | Bout | D2 | D1 |
| 0 | **0** | **0** | **0** | **0** | **0** | **0** |
| 0 | **0** | **0** | **1** | **1** | **1** | **0** |
| 0 | **0** | **1** | **0** | **1** | **1** | **1** |
| 0 | **0** | **1** | **1** | **1** | **0** | **1** |
| 0 | **1** | **0** | **0** | **0** | **1** | **0** |
| 0 | **1** | **0** | **1** | **0** | **0** | **0** |
| 0 | **1** | **1** | **0** | **0** | **0** | **1** |
| 0 | **1** | **1** | **1** | **1** | **1** | **1** |
| 1 | **0** | **0** | **0** | **0** | **0** | **1** |
| 1 | **0** | **0** | **1** | **1** | **1** | **1** |
| 1 | **0** | **1** | **0** | **0** | **0** | **0** |
| 1 | **0** | **1** | **1** | **1** | **1** | **0** |
| 1 | **1** | **0** | **0** | **0** | **1** | **1** |
| 1 | **1** | **0** | **1** | **0** | **0** | **1** |
| 1 | **1** | **1** | **0** | **0** | **1** | **0** |
| 1 | **1** | **1** | **1** | **0** | **0** | **0** |

**Post-Lab Task 1 Circuit Diagram:**

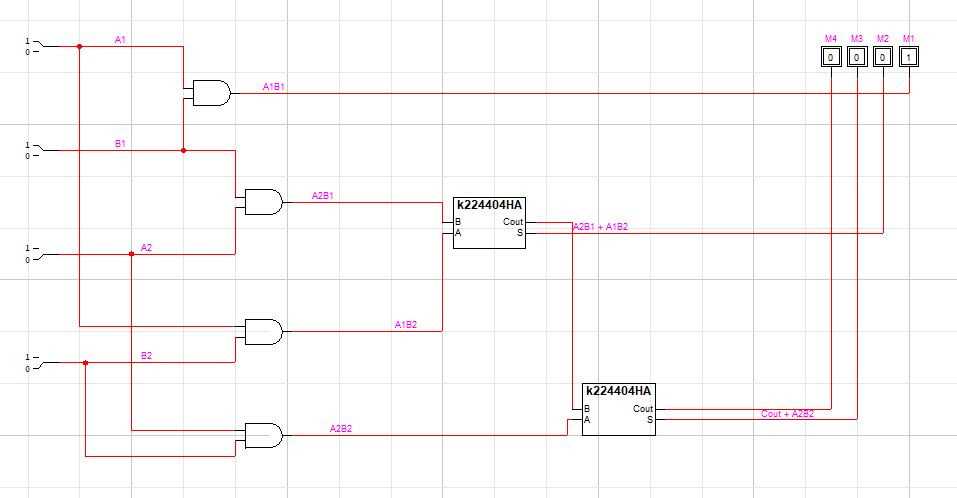


**Post-Lab Task 2 Truth Table:**

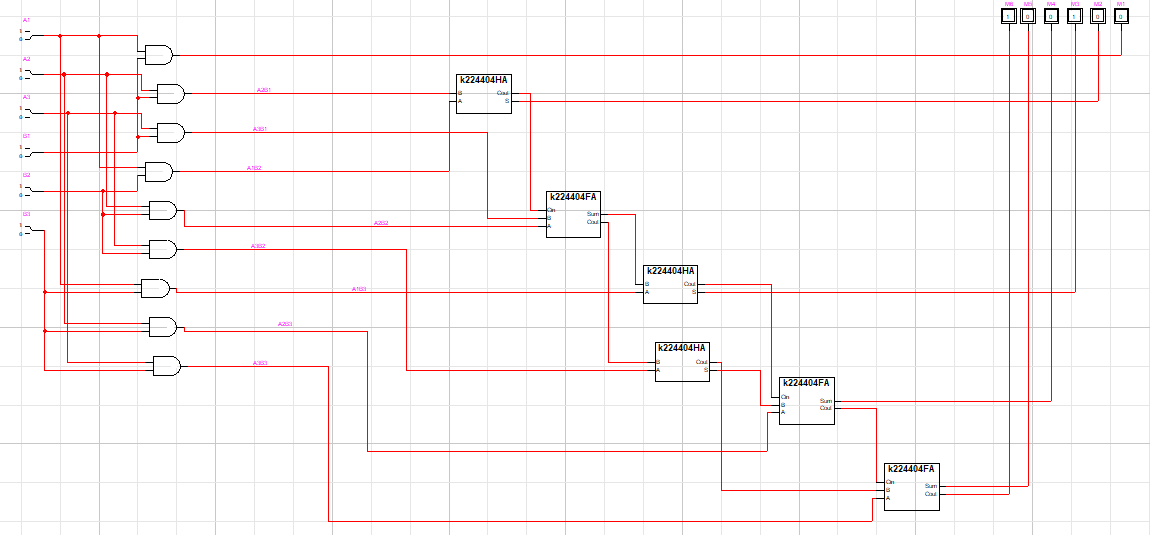
|  |  |
| --- | --- |
| INPUTS | OUTPUTS |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| A2 | A1 | B2 | B1 | Cout | M3 | M2 | M1 |
| 0 | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| 0 | **0** | **0** | **1** | **0** | **0** | **0** | **0** |
| 0 | **0** | **1** | **0** | **0** | **0** | **0** | **0** |
| 0 | **0** | **1** | **1** | **0** | **0** | **0** | **0** |
| 0 | **1** | **0** | **0** | **0** | **0** | **0** | **0** |
| 0 | **1** | **0** | **1** | **0** | **0** | **0** | **1** |
| 0 | **1** | **1** | **0** | **0** | **0** | **1** | **0** |
| 0 | **1** | **1** | **1** | **0** | **0** | **1** | **1** |
| 1 | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| 1 | **0** | **0** | **1** | **0** | **0** | **1** | **0** |
| 1 | **0** | **1** | **0** | **0** | **1** | **0** | **0** |
| 1 | **0** | **1** | **1** | **0** | **1** | **1** | **0** |
| 1 | **1** | **0** | **0** | **0** | **0** | **0** | **0** |
| 1 | **1** | **0** | **1** | **0** | **0** | **1** | **1** |
| 1 | **1** | **1** | **0** | **0** | **1** | **1** | **0** |
| 1 | **1** | **1** | **1** | **1** | **0** | **0** | **1** |

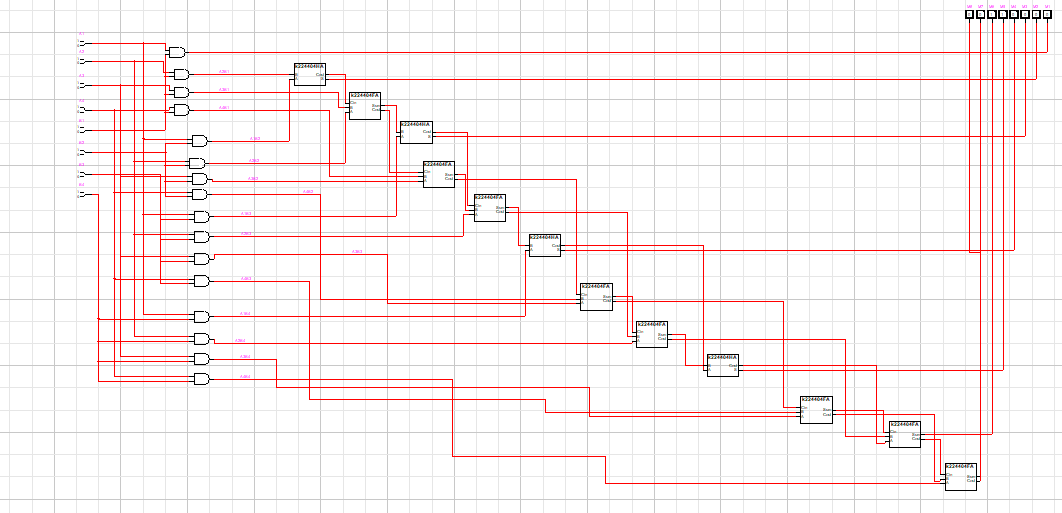
**Post-Lab Task 2 Circuit Diagram:**



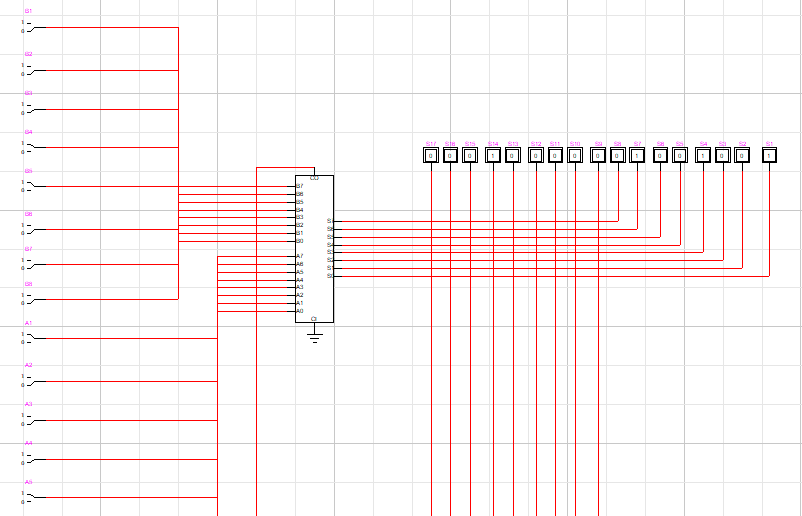
**Post-Lab Task 3 Circuit Diagram:**

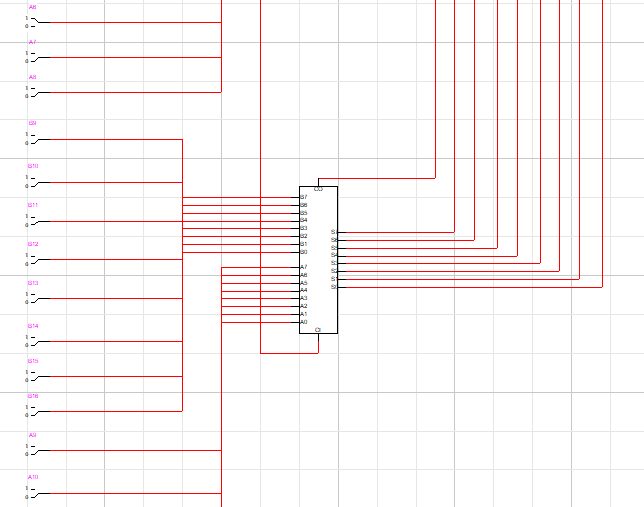


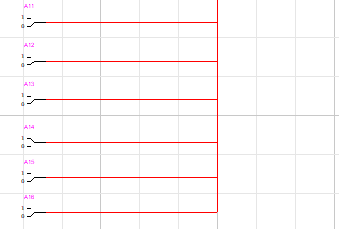
**Post-Lab Task 4 Circuit Diagram:**



**Post-Lab Task 5 Circuit Diagram:**







|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A-Binary | A-Decimal | B-Binary | B-Decimal | Output-Binary | Output-Decimal |
| 0010000000110001 | 8241 | 0000000000011000 | 24 | 00010000001001001 | 8265 |
| 0001110011111101 | 7421 | 0000000000011000 | 24 | 00001110100010101 | 7445 |
| 0001100101010010 | 6482 | 0000000000011000 | 24 | 00001100101101010 | 6506 |